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B Bailey, R Klein, S Leef - Publication pending - newit.gsu.unibel.by

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B Bailey, D Gajski - PROC INT SYMP SYST SYNTH PROC. pp. 69-74. 2001, 2001 - doi.ieeecomputersociety.org

... **Brian Bailey** Mentor Graphics Corp. ... This paper is intended to relate RTL theory and practice with RTL modeling and synthesis/**simulation** issues. ...Cited by 5 - [Web Search](#) - [portal.acm.org](#) - [ieeexplore.ieee.org](#) - [sigda.org](#) - [all 8 versions »](#)Formal verification-prove it or pitch it

R Gupta, S Rawat, S Shukla, B Bailey, D Beece, M ... - Proceedings of the 40th conference on Design automation, 2003 - portal.acm.org

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M Fujita, C Pixley, J O'Leary, F Somenzi - doi.ieeecomputersociety.org

... Panelists: **Brian Bailey**, Mentor Graphics Corp., Dan Beece, IBM Corp ... Despite a number of solid advances in **simulation** and verification techniques over the last ...[Web Search](#) - [ieeexplore.ieee.org](#) - [csdl.computer.org](#) - [dac.com](#) - [all 9 versions »](#)PANEL: HARDWARE/SOFTWARE CO-VERIFICATION

M Kenefick, PR Counsel, CA Los Gatos - doi.ieeecomputersociety.org

... **Brian Bailey**, Mentor Graphics, Wilsonville, OR ... tools are limited to a single abstraction of software and in most cases a single hardware **simulation** session. ...[Web Search](#) - [csdl.computer.org](#) - [sigda.org](#) - [acm.org](#) - [all 7 versions »](#)October, 8th & 9th ZOO3

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... have found, except post silicon." He added: "Dynamic **simulation** is still an ... that are limited to relatively small blocks, **Brian Bailey**, chief technologist ...[Web Search](#)FORMAL VERIFICATION: PROVE IT OR PITCH IT

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G FREYTAG, R SHANKAR - cvs.fau.edu

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G Smith, P Paulin, R Fordham, P Hardee, B Bailey - [portal.acm.org](#)

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R Goering, EE Times - EE Times - [eedesign.com](#)

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